ABSTRACT OF THE DISCLOSURE

A ferroelectric memory device includes memory cells, a memory cell block, a sense amplifier, a precharge circuit, a bit line drive circuit, and a plate line drive circuit. Each of the memory cells has a cell transistor and a ferroelectric capacitor in between a source and drain of the cell transistor. The memory cell block includes the memory cells that are series connected between a bit line via a block select transistor and a plate line. The sense amplifier amplifies data read out from the memory cell, and generates one of a first potential and a second potential higher than the first potential in accordance with the read-out data. The precharge circuit precharges the bit line at a third potential that is higher than the first potential and lower than the second potential. The bit line drive circuit sets the bit line at a fourth potential.